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Numerical Analysis of the Effect of the Step-Coverage on the Parasitic Capacitance

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In this paper, we report our numerical study on the effect of the step-coverage structure on the parasitic capacitances in the LC cell. We analyzed the capacitances of the TN mode LC cell by using the 3D-FEM numerical simulator, TechWiz LCD. In order to calculate the parasitic capacitance, we employed the finite element method (FEM) and the energy method. In the case of the capacitances between the data line and the gate line, we found that the capacitance of the planarized structure is about 2.7 times as large as the capacitance of structure generated with the step-coverage. Our theoretical study revealed that an accurate structure generation is very critical to exactly calculate the parasitic capacitance.

Keywords: 3D-FEM; energy method; parasitic capacitance; simulation; step-coverage; TechWiz LCD

I. INTRODUCTION

Recently, it seems that thin film transistor liquid crystal display (TFT-LCD) is successfully penetrating into the large-area flat panel display (FPD-TV) market as well as the mobile display market. Compared to other competing FPD-TVs, LCD-TVs have many advantages such as high resolution, light weight, slim size, low power consumption, and so on.

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As the panel size of TFT-LCD increases, the unit cell size also increase and therefore the capacitance of the data line and the gate line increases tremendously [1]. The capacitance induces a signal delay, which deteriorates the image quality. To predict the signal delay, it is necessary to calculate the capacitance between the electrodes.

In order to calculate the parasitic capacitance, we employed the finite element method and the energy method [2–3]. We used three parameters which are permittivity, thickness of material and the location of an electrode [4]. To obtain an exact capacitance through the numerical simulation, an accurate structure generation, more particularly, the exact definition of electrode is very crucial. In this paper, we report our comparative study on the capacitance of a structure with taking the step-coverage into account with the simple planarized structure.

II. SIMULATION CONDITION

In this work, we choose a TN mode LC cell as a test vehicle. Table 1 shows the stack information for 3D structure generation. Figure 1 shows the layout of TN mode LC cell used in this simulation. The thickness of the gate line and the data line are designed 0.2 μm. The thickness of the pixel electrode and the common electrode are designed 0.05 μm. The insulator layer was inserted between the electrodes.

TABLE 1 Stack Information for 3D Structure Generation

Zone	Material	Thickness	Planarize	
			Case A	Case B
Top glass	GLASS	50.00 μm	NO	NO
Black Matrix	ALUMINUM	0.20 μm	NO	NO
Insulator	OXIDE	0.21 μm	YES	YES
Common	ITO	0.05 μm	NO	NO
Insulator	OXIDE	0.10 μm	NO	YES
LC	ZLI-4792	4.00 μm	NO	NO
Insulator	OXIDE	0.10 μm	NO	YES
Pixel	ITO	0.05 μm	NO	NO
Insulator	OXIDE	0.30 μm	NO	YES
Data Line	ALUMINUM	0.20 μm	NO	NO
Insulator	OXIDE	0.30 μm	NO	YES
Gate Line	ALUMINUM	0.20 μm	NO	NO
Bottom Glass	GLASS	50.00 μm	NO	NO

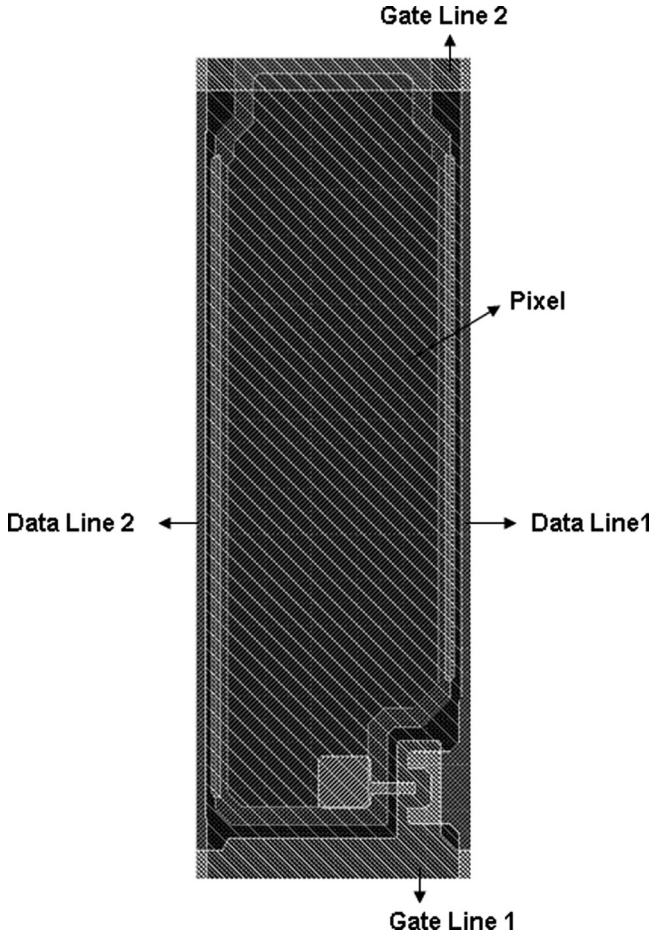

FIGURE 1 A schematic diagram illustrating the layout of TN cell.

The thickness of the top glass and the bottom glass are 50 μm. With the stack information of Table 1, Case A is the structure taking the step-coverage into account. The taper angle is assumed to be 45 degrees. Compared to case A, case B is the case with the planarized insulator layer above the electrode. The other conditions of case B are equal to case A.

The voltage condition of each electrode is shown in Table 2. In order to calculate capacitance more accurately, we divided data lines into data line 1 and data line 2 while the gate lines are divided into gate line 1 and gate line 2, respectively. The gate line 1 and the gate line

TABLE 2 Voltage Condition of each Electrode

Electrode	Voltage [V]
Gate Line 1	–7.0
Gate Line 2	–7.0
Data Line 1	6.5
Data Line 2	6.5
Common Electrode	6.5
Pisxel Electrode	13.0

2 are tied to $-7\,\mathrm{V}$. The data line 1, the data line 2 and the common electrode were tied to 6.5 V. The pixel electrode is fixed at 13 V. For an LC material, ZLI-4792 is selected. The cell size of the structure is assumed to be $9\,\mu\mathrm{m} \times 279\,\mu\mathrm{m}$.

III. CAPACITANCE MODEL

In the cell structure, the energy method was used for calculating the parasitic capacitance. The electric energy W that is stored in a linear capacitor can be expressed by its voltage V:

$$W = \frac{1}{2}CV^2$$

This gives the following for the capacitance,

$$C = \frac{2W}{V^2}$$

The energy W can also be derived from the electric field in the interior of the dielectrics (V_D)

$$W = \frac{1}{2}\int_{V_D} \vec{E}\vec{D}\,dV = \frac{1}{2}\int_{V_D} \varepsilon\left|\vec{E}\right|^2 dV$$

$$\vec{E} = -\nabla\phi$$

There are the energy method and the charge integral method for calculating the capacitance. Both the methods require the numeric calculation of the electric field. However, the charge integral method only needs the field at the conductor surfaces and has no consideration for the multi-dielectrics, whereas the whole domain is required for the energy method.

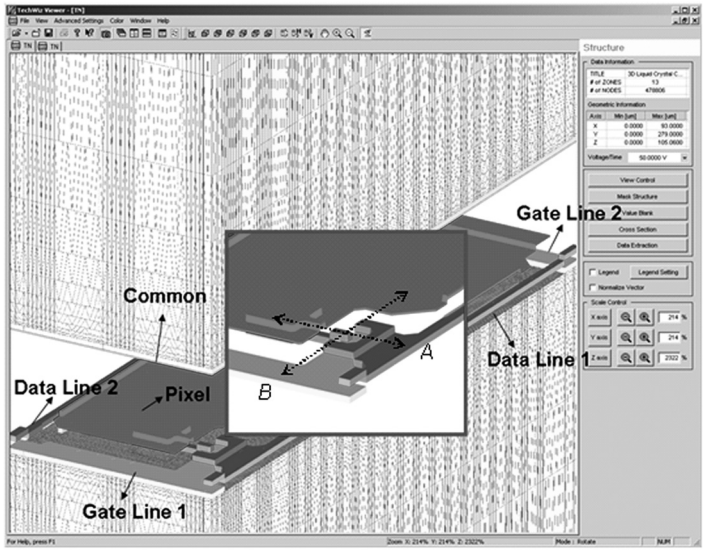

FIGURE 2 A view showing the 3D structure of the case A considering the step-coverage.

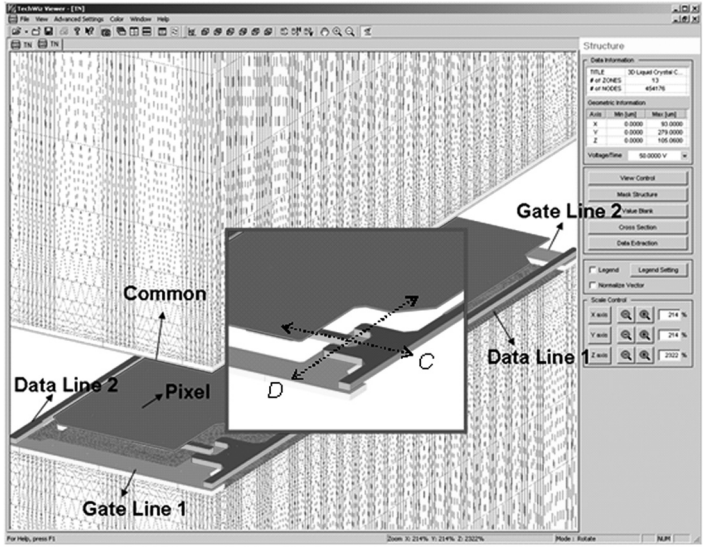

FIGURE 3 A plot showing the 3D structure of the case B with a planar structure.

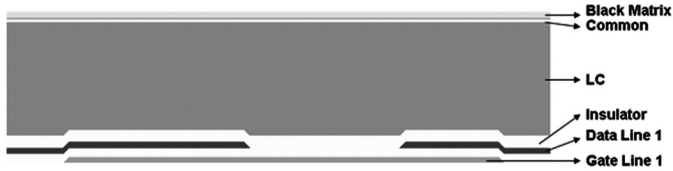

FIGURE 4 A cross-sectional view taken along the direction A of Figure 2.

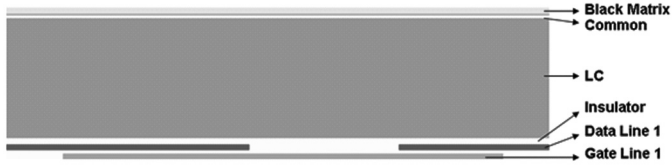

FIGURE 5 A cross-sectional view taken along the direction C of Figure 3.

IV. SIMULATION AND RESULTS

Figures 2 and 3 are schematic diagrams illustrating the structural view of case A with the step-coverage and case B with planar structure, respectively.

Figures 4 and 5 are cross-sectional views illustrating the structure extracted along the direction A of Figure 2 and along the direction C of Figure 3, respectively. As shown in Figures 4 and 5, the thickness of the insulator layer between the gate line and the data line and between the data line and the pixel electrode is different from each other.

Figures 6 and 7 are schematic diagrams illustrating the cross-sectional structure extracted along the direction B of Figure 2 and

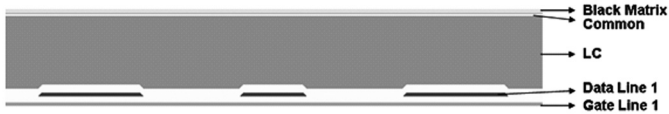

FIGURE 6 A cross-sectional view taken along the direction B of Figure 2.

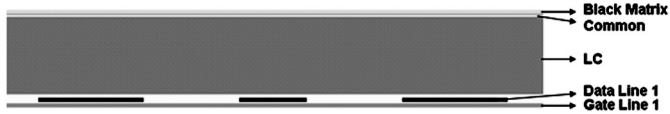

FIGURE 7 A cross-sectional view taken along the direction D of Figure 3.

TABLE 3 Parasitic Capacitance of the Case A and the Case B

Capacitance	Case A (F)	Case B (F)
$C_{G1\text{-}D1}$	$\mathbf{3.49084 \times 10^{-14}}$	$\mathbf{9.47678 \times 10^{-14}}$
$C_{G1\text{-}D2}$	$\mathbf{6.10629 \times 10^{-15}}$	$\mathbf{1.63635 \times 10^{-14}}$
$C_{G1\text{-}C}$	1.66686×10^{-14}	1.72859×10^{-14}
$C_{G1\text{-}P}$	$\mathbf{9.86441 \times 10^{-15}}$	$\mathbf{1.75825 \times 10^{-14}}$
$C_{G2\text{-}D1}$	$\mathbf{5.75501 \times 10^{-15}}$	$\mathbf{1.56782 \times 10^{-14}}$
$C_{G2\text{-}D2}$	$\mathbf{6.81814 \times 10^{-15}}$	$\mathbf{1.83828 \times 10^{-14}}$
$C_{G2\text{-}C}$	2.05775×10^{-15}	2.21384×10^{-15}
$C_{G2\text{-}P}$	$\mathbf{5.05734 \times 10^{-14}}$	$\mathbf{7.25878 \times 10^{-14}}$
$C_{D1\text{-}C}$	1.10425×10^{-14}	1.09220×10^{-14}
$C_{D2\text{-}C}$	8.35169×10^{-15}	8.38678×10^{-15}
$C_{P\text{-}D1}$	4.59891×10^{-15}	4.68147×10^{-15}
$C_{P\text{-}D2}$	4.85945×10^{-15}	5.00231×10^{-15}
$C_{P\text{-}C}$	2.85422×10^{-13}	2.86030×10^{-13}

along the direction D of Figure 3, respectively. Compared to the case A, the thickness of insulator layer between the gate line, the data line and the pixel electrode is irregular in case B.

Table 3 shows the simulation result of the parasitic capacitance between the electrodes in each case. In Table 3, $C_{G1\text{-}D1}$, $C_{G1\text{-}D2}$, $C_{G1\text{-}P}$, $C_{G1\text{-}C}$, $C_{G2\text{-}D1}$, $C_{G2\text{-}D2}$, $C_{G2\text{-}P}$, $C_{G2\text{-}C}$, $C_{D1\text{-}P}$, $C_{D2\text{-}P}$, $C_{C\text{-}D1}$, $C_{C\text{-}D2}$ and $C_{P\text{-}C}$ represent the capacitances between the gate line 1, the gate line 2, the data line 1, the data line 2, the pixel electrode and the common electrode, respectively. For instance, $C_{G2\text{-}D1}$ indicates the capacitance between the gate line 2 and data line 1.

Referring to Table 3, we can see that $C_{G1\text{-}P}$, the capacitance of the case B is about 1.78 times larger than the capacitance of the case A, while $C_{G2\text{-}P}$ of the case B is about 1.44 times as large as $C_{G2\text{-}P}$ of the case A. There exists a great difference in the capacitance values between the gate line, the data line and the pixel electrode. The method of the structure generation greatly influences the thickness of the insulator layer and the area of each electrode. Even the minor difference in the structure results in a significant impact on the capacitance result. The capacitances between the common electrode and the other electrodes except for the above-mentioned capacitances are almost same.

V. CONCLUSION

We have studied the effect of the step-coverage on the capacitance by numerical simulation. We investigated two cases where the structure

of the case A includes the step-coverage while the structure of case B is just a planar structure. The capacitance between the gate line and the data line was of the case B is about 2.7 times larger than the capacitance of the case A. Our simulation revealed that it is very crucial to be able to implement even the minor structural change like step coverage at the step of structural generation for FEM calculation if we would like to obtain an accurate capacitive values for the whole LCD panel simulation.

REFERENCES

[1] Kwon, O. K., *et al*. (2005). *SID '05 Digest*, 1856.
[2] Uchida, Y., *et al*. (2003). *ESSDERC '03*, 453.
[3] Stach, A., *et al*. (1997). *Proceedings IASTED Intl. Conference on Modeling, Identification and Control*, 16.
[4] Arora, N. D., *et al*. (1996). IEEE Trans. *Computer-Aided Design*, *15*, 58.
[5] User's Guide of TechWiz LCD 2005 (2005). *Sanayi System Co., Ltd.* Technical User's Manual Techwiz LCD 2006, Sanayi System Co. Ltd.